IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

MEDIATEK, INC., Plaintiff, v. SANYO ELECTRIC CO., LTD. AND SANYO NORTH AMERICA CORPORATION, Defendants.	Civil Action No. No. 6:05cv323 (LED) **Oral Argument Requested**

DEFENDANTS' RESPONSIVE MARKMAN BRIEF

I. INTRODUCTION

Pursuant to Local Patent Rule 4-5(b) and the Court's Docket Control Order, defendants Sanyo Electric Co., Ltd. and Sanyo North America (collectively "Sanyo") respectfully submit this brief in response to plaintiff MediaTek's Opening Claim Construction Brief that was filed on August 31, 2006. This brief sets forth defendants' proposed constructions of disputed claim terms, and explains why those constructions are proper and why MediaTek's are unsound in view of the evidence. For the Court's convenience, a summary of both parties' proposed claim constructions is provided at Exhibit 1.

As we explain below, Sanyo's proposed construction of the disputed claim terms is fully consistent with the intrinsic evidence of the patents-in-suit – that is, the language of the claims themselves, the patent specifications and their prosecution histories. Sanyo's proposed construction also is fully consistent with the stated purpose of the claimed inventions.

The root of the claim construction disputes before the Court is MediaTek's effort to read narrowly written claims more broadly. While MediaTek has modified many of the constructions it advanced in the Joint Claim Construction Statement, the problems remain. Many of the claim terms the Court is being asked to construe are means-plus-function terms. MediaTek acknowledges the rules for constructing claims written in accordance with 35 U.S.C. § 112(6), but is unable to follow them. In particular, MediaTek's proposed constructions repeatedly ignore the structure disclosed in the specification. MediaTek's construction of other terms is likewise infirm. MediaTek's constructions are based on lawyer's arguments, not evidence. MediaTek reads the claims in a vacuum, without regard to what is said in the specification of the patents or other representations made to the Patent Office ("PTO") during prosecution.

Indeed, it is noteworthy that in this case, Sanyo was unable to take any claim construction discovery from MediaTek. MediaTek bought the patents-in-suit. But it claims not to know the whereabouts of the inventors. It claims not to have any invention records. In fact, MediaTek has hardly any relevant documents at all (in the seven months of discovery to date, MediaTek has produced roughly 20,000 pages of documents, which includes the file histories of the three patents in suit). MediaTek apparently believes that this provides the opportunity to rewrite history. But *Markman*, *Phillips* and other cases do not permit this approach. These cases require proper use of the intrinsic evidence.

The Court should adopt the constructions proposed by Sanyo as detailed below.[1]

II. THE LAW OF CLAIM CONSTRUCTION

Before undertaking to explain how various claim terms should be construed, Sanyo wishes to counter MediaTek's one-sided discussion of claim construction law.

A. Claims Must Be Read In View Of The Specification, Not In Vacuum

The Federal Circuit recently affirmed the central role the specification of a patent plays in interpreting disputed claim terms. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Claims "do not stand alone" and "'***must be read in view of the specification***, of which they are a part.'"[2] *Id*. at 1315 (citation omitted). The specification is the "primary basis for construing the claims" because it provides the ***context*** for the claims. *See id.* at 1315-16 (internal citations omitted).

[1] Consistent with the affirmative defenses pled in defendants' Answer To Second Amended Complaint, many claim terms addressed in this brief do not comply with the requirements of 35 U.S.C. § 112 and thus are invalid. Defendants do not address the invalidity issues here but reserve them for resolution at a later date.

[2] Unless otherwise stated, all emphasis in this brief is added.

MediaTek would have the Court believe that the specification may be used to construe claims in only exceptional circumstances. According to MediaTek, claims must be construed simply by looking at the claim language and determining the ordinary meaning in a vacuum far removed from the context of the patent. That is not the law. "***[T]he specification is always highly relevant*** to the claim construction analysis. Usually, it is dispositive; it is ***the single best guide to the meaning*** of a disputed term." *Vitronics Corp.* v. *Conceptronics, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Phillips*, 415 F.3d at 1315; *see also Maurice Mitchell Innovations* v. *Intel Corp.,* No. 2:04-cv-450, slip op. at 3 (E.D. Tex., June 21, 2006).

The specification is usually dispositive because "a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope." *Mitchell Innovations*, slip op. at 3; *Phillips*, 415 F.3d at 1316. In such situations, the inventor's lexicography governs. *Id.* Also, "the specification may resolve ambiguous claim terms 'where the ordinary and accustomed meaning of the words used in the claim lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone.'" *Mitchell Innovations*, slip op. at 3; *Teleflex, Inc.* v. *Ficosa N. Am. Corp*., 299 F.3d 1313, 1325 (Fed. Cir. 2002).

Therefore, courts should "give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the ***context of the entire patent***." *Mitchell Innovations*, slip op. at 2 (emphasis added); *Phillips*, 415 F.3d at 1312-13. "The construction that stays true to the claim language and most naturally ***aligns with the patent's description of the invention*** will be, in the end, the ***correct construction***." *Id.* at 1316 (internal citations omitted).

MediaTek correctly notes that ordinary claims should not be interpreted to limit them to the embodiments disclosed in the specification.[3] However, most of the time, "***upon reading the specification***," it will become clear "whether the patentee is setting out specific examples of the invention to accomplish those goals, or whether the patentee instead intends for the claims and the embodiments in the specification to be strictly coextensive." *Phillips*, 415 F.3d at 1323.

B. A Means-Plus-Function Limitation, Like Any Limitation, Has No Meaning Outside Of The Specification

As MediaTek points out, some of the claim limitations are in means-plus-function format and require special treatment by the Court under 35 U.S.C. §112(6). But, as with any claim limitation, the specification is the primary basis for construing means-plus-function limitations. Means-plus-function limitations are construed by first determining their function and then consulting the specification to identify the corresponding structure that performs the function. *Medtronic, Inc.* v. *Advanced Cardiovascular Sys.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001); *Lockheed Martin Corp.* v. *Space Sys./Loral, Inc.*, 324 F.3d 1308, 1319 (Fed. Cir. 2003); *Mitchell Innovations*, slip op. at 4.

"A 'structure disclosed in the specification is "corresponding" structure only if the ***specification or prosecution history clearly links or associates that structure to the function*** recited in the claim.'" *Id.* (citation omitted). "Moreover, the focus of the 'corresponding structure' inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is 'clearly linked or associated with the [recited] function.'" *Id.* at 4-5 (citation omitted)

[3] Means-plus-function claims are interpreted differently, as set forth *infra*.

C. Claims Must Be Interpreted In Light Of The Purpose Of The Invention

MediaTek would also have the Court believe that the purpose of a patented invention is completely irrelevant for the purpose of claim construction. Not so. "[C]laim[s] ***must*** be interpreted in light of the teachings of the ***written description and purpose of the invention*** described therein." *Apple Computer, Inc.* v. *Articulate Sys., Inc.*, 234 F.3d 14, 25 (Fed. Cir. 2000). A claim construction that eviscerates the very purpose of the invention cannot stand. *Howmedica Osteonics Corp*. v. *Tranquil Prospects, Ltd*., 401 F.3d 1367, 1372-73 (Fed. Cir. 2005).

D. The Intrinsic Evidence Serves A Public Notice Function And Cannot Be Ignored

Like the specification, the prosecution history also provides "the proper context for claim construction" and courts must consult it so as "to ***exclude any interpretation that was disclaimed during prosecution***." *Mitchell Innovations*, slip op. at 3; *Phillips*, 415 F.3d at 1317 (internal citations omitted).

But MediaTek would have the Court believe that there is no need to consult the prosecution history as long as the term's ordinary meaning is ascertainable in a vacuum without any context. That, however, is the methodology for arriving at a dictionary definition, not a definition of a patent claim term. And even a dictionary definition cannot be accepted on its own because "the intrinsic record must always be consulted to identify which of the different possible dictionary meanings is ***most consistent with the use of the words by the inventor***." *Brookhill-Wilk 1, LLC* v. *Intuitive Surgical, Inc*., 334 F.3d 1294, 1300 (Fed. Cir. 2003).

This is because, the intrinsic record, including the specification and the prosecution history, "constitute the public record of the patentee's claim, a record on which the public is entitled to rely." *Vitronics*, 90 F.3d at 1583. This "notice function is critical because it

provides competitors with the necessary information upon which they can rely to shape their behavior in the marketplace." *Litton Sys., Inc.* v. *Honeywell, Inc.,* 145 F.3d 1472, 1474 (Fed. Cir. 1998). Accordingly, the intrinsic record cannot be ignored while construing the claims.

III. THE PATENTS-IN-SUIT

MediaTek has asserted three patents in this case. Each has claim terms that need to be construed.

A. The '819 Patent

U.S. Patent No. 5,867,819 ("'819 patent") relates broadly to devices called audio decoders. (MT Ex. A).[4] Audio decoders convert compressed digital audio data into uncompressed digital data that can then be converted into analog signals for amplifiers or speakers. The '819 patent is related to very specific hardware for converting this data into audio signals. This patent, in particular, is directed to hardware that converts audio data recorded for many speakers into audio signals for fewer speakers as well as using less memory than previous systems. (*See* Sanyo's Tutorial submitted to the Court for more detail).

The '819 patent describes down mixing processes for converting sound from many channels to fewer channels. The '819 patent describes specific equations to be used for down mixing.

The '819 patent explains that prior art systems down mixed time domain audio signals after they were decoded from compressed frequency domain data. This prior art down mixing occurred as the last step before the digital audio signals were sent to be converted into analog form for the speaker or amplifier. Performing down mixing in this order required additional computer memory to store data from each channel between the steps of decoding the

[4] "MT Ex. _" refers to the exhibit attached to MediaTek's Opening Claim Construction Brief.

data and down mixing the data. The ‘819 patent addresses the problem of excess memory use by various specific down mixing configurations that reduce memory requirements.

The ‘819 patent describes four different ways of down mixing. These configurations are important, because all of the asserted claims of the ‘819 patent include means-plus-function elements such as down mixing means. Different claims refer to different embodiments shown in the specification. Therefore, a claim term such as down mixing means needs to be construed differently depending on which claim is being construed.

The first type of down mixing described in the patent is down mixing the digital frequency domain data before decoding it into a time domain audio signal, as shown in figure 8. (MT Ex. A Fig. 8). This configuration of down mixing reduces the memory requirements of the system.

The second way down mixing is described involves the time domain audio signal being down mixed after it has been decoded from the frequency domain data. This is described as differing from the prior art shown in figure 6, because computer memory is reduced in size and moved to a different point in the circuit. (MT Ex. A 11:28-31, 11:47-55).

The third way down mixing occurs in the ‘819 patent, like the second, is that down mixing occurs after the frequency domain data is decoded into time domain audio data. However, in this configuration, the computer memory is not placed differently or changed from the prior art configuration. (MT Ex. A (*compare* element 39 of Fig. 6 *to* element 6 in Fig. 12)).

The fourth way to down mix, in the ‘819 patent, is also a variation of the second. However, in the fourth configuration, the time domain audio signal is split before decoding is complete. (MT Ex. A 14:45-65). This is shown in figure 15. Approximately half of the audio data is decoded in element 11 before down mixing occurs. The remaining data is down mixed

before being decoded in element 15. This operation requires two down mixing circuits and two decoder or window applying operating circuits.

As stated, the ‘819 patent describes converting digital audio recordings between the frequency domain and the time domain. Frequency domain and time domain are two different mathematical representations of sound waves. As mentioned, frequency domain is often used to store compressed data, while time domain is used to play back audio signals. Because of this, frequency domain and time domain data should not be mixed together.

To convert from time domain to frequency domain, blocks of sound data are fed into a special equation called a modified discrete cosine transform, or MDCT. (MT Ex. A 1:45-48). The MDCT is an unusual equation because it has half as many outputs as inputs. Converting from frequency domain to time domain is accomplished by feeding blocks of sound data in frequency domain format into a different, but equally special, equation. This equation is called an inverse modified discrete cosine transform, or IMDCT. (MT Ex. A 3:42-58). The IMDCT is able to convert the data back to the form it had before it was fed through the MDCT. As part of this conversion back, the IMDCT is able to output twice as many outputs as inputs.

The ‘819 patent also discusses something called a window function. (MT Ex. A 1:58-65). A window function is used to blend overlapping blocks of data together into a continuous stream of sound. Without the use of a window function, a freshly converted sound wave at the end of block number zero might not match the freshly converted sound wave at the beginning of block number two. Likewise, the freshly converted sound wave at the end of block number one might not match the freshly converted sound wave at the beginning of block number three, and so on. Because of this, the ‘819 patent talks about using a window function to

reconstruct the sound waves. Figure 2 of the patent shows a window function that looks very similar to two quarter circles attached by a straight line.

B. The '486 Patent

U.S. Patent No. 6,118,486 ("'486 patent") describes a method and circuitry by which a digital television accepts input video signals in multiple formats and processes them to be displayed in a format compatible with the television display. (MT Ex. B). The patent describes a specific and simple way of generating a raster clock used in displaying the video, thereby reducing the circuitry needed to operate the television. The patent also describes a specific and simple way of processing the multiple formats of input video signals for display. (*See* Sanyo's Tutorial submitted to the Court for more detail).

The ***sole*** purpose of the invention is to make the circuitry simpler and cheaper:

> Specifically, the inventor recognized that ***considerable cost savings may be achieved*** in a multiple video format system by utilizing a raster (pixel) clock and horizontal and vertical deflection frequencies that are easily derived from the 27 MHz system clock used for receiver synchronization in an MPEG-like video processing system. Moreover, the inventor recognized that ***further cost savings may be achieved by*** selecting, for use by a display device, a single horizontal scanning frequency and adapting the video format of a received video signal to a format defined by, e.g., the selected horizontal scanning frequency and the resolution of the display device. (MT Ex. B at 2:37-48).

The simplicity and cost-savings of the described system are repeatedly reinforced throughout the specification. (MT Ex. B at 2:11-17; 2:37-53; 7:55-58; 8:6-8; 8:64-66; 12:63-67). Indeed, simplicity and cost-effectiveness is the very reason the inventor came up with the '486 invention:

> Therefore, ***a need exists in the art for a cost-effective video processing system*** suitable for use in, e.g., a multiple format television receiver. It is also seen to be desirable to provide a video system that advantageously utilizes display timing processing that, unlike prior art front-end video processing systems, comprehensively ***reduces total system cost and complexity***. (*Id*. at 2:11-17).

The '486 patent teaches making the video processing system ***simpler and cheaper*** in four ways that are relevant to the claim construction issues in this case:

- using a single clock circuit to generate both the system clock and the raster clock, rather than having two separate clock circuits.
- using non-standard frequencies for the raster clock instead of the standard frequency of 74.25 MHz.
- using system and raster clocks that are simple ratios of one another and easily derived from one another.
- using a fixed horizontal deflection frequency for the display device and simple resizing or adjusting of the format of the input video.

As shown in Figure 1, the only schematic illustration of the invention in the '486 patent, a single clock circuit 110 generates both the system clock f_{SYS} and the raster clock f_{RAST}. And the input for generating both these clocks is the program clock reference signal (PCR).

The clock circuit 110, as shown in Figure 1, consists of one phase locked loop (PLL) 112, one voltage controlled oscillator (VCO) 114, and one frequency scaler 116. (MT Ex. B at 4:36-38). The clock circuit outputs two signals – the system clock f_{SYS} and the raster clock $f_{RAST.}$ This clock circuit is a single loop and is self-correcting based on a comparison of the PCR and the output signal f_{SYS}. Because the frequency scaler is located inside the single loop, both clocks are essentially generated simultaneously by the clock circuit. Prior art systems typically used one clock circuit to generate the system clock and a second clock circuit to generate the raster clock. Having separate clock circuits to generate the system and raster clock increases the amount of circuitry, thereby increasing the overall system complexity and cost.

In Figure 1, the same clock circuit can be used to generate both the system and raster clocks because, according to the patent, the clocks are "***easily derived***" from one another, i.e., simple ratios of one another. For example, a 81MHz raster clock and a 27 MHz system clock can be generated from a single circuit using a 3:1 ratio. The frequency scaler scales one

clock to obtain the second clock. For example, the scaler divides 81MHz by 3 to obtain the 27 MHz clock. Utilizing simple ratios for the clocks simplifies the scaling circuitry. For example, a simple divider can be used to divide 81 MHz to obtain 27 MHz. On the other hand, a 74.25 MHz raster clock requiring a multiplication of 2.75 (11:4 ratio) needs more complex circuitry, which is neither described nor taught by the patent. Prior art systems used relatively more complex circuitry to generate the required raster clocks because their raster clocks were not related to the system clock as simple ratios – the prior art systems typically used the standard 74.25 MHz raster clock.

A related aspect of the system clock being "easily derived" from the raster clock is that the raster clock is of a ***non-standard*** value. The standard raster clock used in HD TVs is 74.25 MHz. 74.25 MHz is not a simple ratio of 27 MHz and accordingly requires complex circuitry to generate it. Prior art systems used standard raster clocks by utilizing a second clock circuit. The patent does not teach or explain anywhere how a 74.25 MHz raster clock can be generated by scaling a 27 MHz system clock. In fact, the patent discusses why the use of non-standard frequencies that are close to the standard frequency is acceptable: "***To reduce system cost and complexity, the DTV receiver 100 of FIG. 1 utilizes a non-standard frequency for raster clock***." (MT Ex. B at 8:6-8).

In terms of processing the format of the input video signal to be compatible with the display device, the patent again teaches ***simplicity and cost reduction***. For example, if the format of the input video is 640 by 480 pixels and the format of the display device is 1920 by 1080 pixels, the system utilizes horizontal and vertical resizers to adjust the format of the input video. To keep it simple, the system adjusts the format by doubling the 480 lines to 960 lines and doubling the 640 pixels per line to 1280. Adjusting the 480 lines exactly to 1080 lines

requires complex circuitry – multiply 480 by 9 and then divide by 4. Further, the patent teaches keeping the ***horizontal deflection frequency of the display device fixed*** regardless of the input video format. Changing the horizontal deflection frequency with the input video as done by prior art systems increases the circuit complexity.

C. The '356 Patent

U.S. Patent No. 5,751,356 ("'356 patent") describes a method and system by which audio and video signals are coded while reducing the load traditionally placed on the processor. (MT Ex. C). The patent describes a system that encodes the input video data (i.e., raw video) and attaches encoding information including header information to the video data as a video header and outputs data number information indicative of a number of the encoded video data. The system includes control means that takes the data number information and the header information which have been removed by the video encoding means and uses them to perform the multiplexing operation that produces the data containing the encoded video and audio data and the system header. (*See* Sanyo's Tutorial submitted to the Court for more detail).

According to the inventor of the '356 patent, the invention is that "the video header information is input directly from the video encoding means for creating the video header information, so that, during the multiplexing operation at high encoding rate, the need for extracting the video header information from a bit stream, **which would impose a heavy load on the processor in the prior art**, can be ***eliminated***, thus reducing the load of the processor." (MT Ex. C at 2:64 – 3:4). Thus, according to the '356 patent inventor, prior art systems created the system header information by processing the video bit stream, while the '356 invention created the system header information by only processing the data number information and the header information without having to process the video bit stream.

The specification describes one, and only one, way to create MPEG 1 and MPEG 2 data files. As shown in figure 1 and described in the specification, the encoder circuit 11 encodes the received video signal and passes attributes, or the like, to the header creation circuit 12. (MT Ex. C at 3:52-58; Fig. 1). Header creation circuit 12 creates GOP headers, sequence headers and picture headers based on the data encoded by the encoder circuit 11. (*Id.* at 4:12-14). "The header creation circuit also determines a bit length of the bit stream, e.g., between the picture headers, that is, a bit length L. The bit length L is stored in the memory 3, together with the sequence headers SH, GOP headers and picture headers, which will be referred to as the video information." (*Id*. at 4:20-25). "The multiplexer circuit 13 then transmits the thus-created MPEG2-based bit stream to the multiplexer circuit 6." (*Id.* 4:17-19).

"More specifically, the processor 4, provided within the multiplexer 7, reads out the video information from the memory 3 and creates the system header information necessary for making a layered system structure. The video information stored in the memory 3 includes header information on the sequence headers SH, GOP headers and picture headers included in the video bit stream of the video signal encoder 1, as well as information on the bit length L of the stream corresponding to one picture and on the encoding rate. The processor 4, on the basis of the video information, determines the multiplexing order of the video and audio data and creates the system header information." (MT Ex. C at 4:51-62).

That is, the controller judges the boundary and issues related commands to the other circuitry. The processor 4 controls the multiplexer circuit 6 with respect to each predetermined video unit. The processor 4 uses the header information to locate the head (i.e., beginning) of each predetermined video unit. It then uses the bit length L to judge the boundary of the predetermined video unit. This combined information allows the processor to determine

how to separate the data stream into meaningful segments. This separation is done by issuing command signals (i.e., the data select signal 9 and a data byte number signal 10) to the multiplexer circuit.

IV. DEFENDANTS' PROPOSED CONSTRUCTIONS

In the following sections, for each term identified in the Joint Claim Construction Statement, Sanyo sets forth its construction. In some instances, where MediaTek modified its construction to something more reasonable than that in the Joint Statement, and in order to narrow the terms needed to be construed, Sanyo does not dispute MediaTek's revised constructions. Where disputes remain, Sanyo sets forth why its construction, and not MediaTek's should be adopted. For the convenience of the Court, Sanyo has reproduced at Exhibit 2 the asserted claims with the disputed limitations set forth in bold-face type. Further, Exhibit 1 provides each of MediaTek's and Sanyo's constructions for the terms identified in the Joint Claim Construction Statement. Where Sanyo does not dispute MediaTek's construction, Sanyo so states.

A. The '819 Patent

The parties agree that each of the '819 patent limitations to be construed is a "means plus function" limitation. (MT Ex. D at 2). Such limitations must be construed pursuant to 35 U.S.C. § 112(6). The process of construing a means plus function limitation is different from the process used to construe other claim limitations. Once a court establishes that a means-plus-function limitation is at issue, it must identify and construe that limitation, thereby determining what the claimed function is, and what structures disclosed in the written description correspond to the 'means' for performing that function. *See supra* at 5.

The parties dispute the construction of four means-plus-function claim terms in the '819 patent.[5]

1. Frequency Domain Down Mixing Means (Claims 1 and 6)

Function

MediaTek's proposed construction for the functions of claims 1 and 6 either reiterates the exact claim language or entirely ignores the recited function.

It is plain from the language of claims 1 and 6, the specification of the '819 patent, the description of equation (4), and Figs. 7 and 8, that the "frequency domain down mixing" must occur in the frequency domain. (MT Ex. A at 8:39-43, 9:23-25, Figs. 7, 8). If this is not true, then the references in the preamble and limitations at issue, to a "plurality of channels in a frequency domain" and "frequency domain down mixing means," are meaningless. But, MediaTek's proposed construction of the function leaves open the possibility that certain of the channels being mixed together might contain time domain audio data. Accordingly, for claim 1, Sanyo proposes the following construction of the function of this limitation in a form that is both true to the claim language and which a jury is more likely to understand:

"processing the frequency domain audio data by mixing multiple channels of frequency domain audio signals into a predetermined number of channels of frequency domain audio signals at a predetermined level ratio."

This construction makes clear which data is being operated upon. Sanyo replaces "processing . . . so as to mix" with "processes . . . by mixing," in an attempt to remove

[5] Sanyo no longer disputes MediaTek's construction of the terms "inverse quantizing means," time base to frequency base converting means," and "window applying means."

complication for the jury's benefit. Sanyo also replaces "plurality" with its ordinary meaning, "multiple."

Claim 6 adds the limitation, "when the length of data block [sic] with respect to the audio signal of at least one channel to be processed is different from the length of the data block with respect to the audio signal of the other channel to be processed, said frequency domain down mixing means eliminates the audio signal of said at least one channel from targets to be mixed." (MT Ex. A at 19:37-44). Sanyo proposes that the Court construe the added function of the claim 6 "frequency domain down mixing means" as follows:

"eliminating the audio data of channel(s) with differing conversion block lengths from the down mixing process."

This proposed function sets forth the ordinary meaning of the claim.

Structure

MediaTek's proposed structure for ***claim 1*** lacks most of the structure disclosed in the patent. The '819 patent sets forth no structure for performing the function of ***claim 6.*** "A means-plus-function claim encompasses all structure in the specification corresponding to that element and equivalent structures." *Micro Chem., Inc.* v. *Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999). MediaTek identifies specific structure from the specification related to claim 1. (MT Br. 13 ("Figure 7, element 40 and Figure 8, element 101")) But, MediaTek then ignores the specification when it requests that the Court identify a generic "down mixing circuit" as the required structure. (*Id.* at 14). Sanyo respectfully requests that the Court identify specific down mixing circuits from the specification, as proposed by Sanyo. Those circuits include specific inputs, input paths, outputs, and output paths that may not be found in a generic circuit, but were purposefully included in the patentees' description of the purported invention. (MT Ex. A at 8:39-46, 9:8-12, Figs. 7, 8).

MediaTek suggests that the Court not identify "equation (4)" as part of the required structure. Equation (4) is a mathematical form of the process implemented by the "frequency domain down mixing means." (MT Ex. A at 9:12-15). The equation specifies that the down mixed signal in the frequency domain (*Y[n]*) is equal to the sum (Σ) of a number of channels (*ch* = 0 [to] *M-1*) of frequency domain input data (*X[ch][n]*); where each channel's data is multiplied by a down mixing coefficient (α*[ch]*). (*Id*. at 9:17-27). This is no different from the claim language directed to mixing "the audio signals [(*X[ch][n]*)] of said plurality of channels [(*ch* = 0 to *M-1*)] into the audio signals [(*Y[n]*)] of a predetermined number of channels at a predetermined level ratio [(α*[ch]*)]." (*Id.* at 18:38-42). Moreover, the '819 patent specifies, "The process to be executed in the frequency domain down mixing circuit 101 is described by the following equation (4)." (*Id.* at 9:12-14). As such, a circuit implementing this equation is part of the structure corresponding to the claimed function.

MediaTek's proposal to exclude the equation is particularly problematic, because the functions identified for claims 1 and 6 include "a predetermined level ratio." A generic down mixing means may not perform the functions related to a "predetermined level ratio." However, where the identified function calls for a "predetermined level ratio," the law requires identification of structure that implements that function. The only structure identified by the '819 patent for this purpose is a circuit implementing equation (4). (MT Ex. A at 9:12-26).

"[T]he corresponding structure for a § 112 ¶ 6 claim for a computer-implemented function is the algorithm disclosed in the specification." *Harris Corp.* v. *Ericsson, Inc.*, 417 F.3d 1241, 1249 (Fed. Cir. 2005); *see WMS Gaming, Inc.* v. *Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999) ("In a means-plus-function claim in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the

general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm."); *accord Tehrani* v. *Hamilton Med., Inc.*, 331 F.3d 1355, 1362 (Fed. Cir. 2003) ("[W]e must remand this case for the district court to determine what algorithm forms part of the structure of the 'means for processing' limitation. . . ."). These algorithms include the equations disclosed in the specification. *Id*. at 1362 ("[on remand], the court should consider whether the algorithm consists solely of the resultant equations . . . or includes the underlying calculations. . . .").

Whether the Court identifies a circuit for implementing equation (4) as corresponding structure or not, that equation remains part of the claimed function and the result is the same. Thus, Sanyo requests that the Court identify the following structure as corresponding to the claim 1 function:

"a frequency domain down mixing circuit as shown in element 40 or Fig. 7, element 101 of Fig. 8, which implements equation (4)."

Finally, the '819 patent does not identify any structure associated with frequency domain down mixing that corresponds to the function of claim 6. (*See e.g.* MT Ex. A at 10:36-43). The patent's discussion of "eliminating" channels with differing block lengths does not associate any structure for "eliminating." (*Id.* at 10:36-48). "[P]ursuant to [35 U.S.C. § 112(6)], structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *B. Braun Med., Inc.* v. *Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). Thus, Sanyo respectfully requests that the Court rule that the patent does not disclose any structure corresponding to the claim 6 function.

2. Frequency Base To Time Base Converting Means (Claims 1, 3, 11, 13 and 16)

Function

For claim 1, having considered MediaTek's arguments and MediaTek's revised proposed construction, Sanyo does not dispute MediaTek's revised construction. Therefore, there is no dispute as to the proposed function of this means in claim 1.

For claim 3, MediaTek was aware of Sanyo's proposed construction,[6] but did not address the language of claim 3, which states, "said frequency base to time base converting means converts the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to the time domain on the basis of the block length information separated by said separating means." (MT Ex. A at 19:1-6). Sanyo has set forth a construction based on the ordinary meaning of this term. Accordingly, because MediaTek chose not to propose a construction, Sanyo respectfully requests that the Court construe this function for claim 3 to have its ordinary meaning as:

"converting frequency domain audio data processed by the 'frequency domain down mixing means' from the frequency domain to time domain based on the block length information separated by the 'separating means.'"

For claim 11, MediaTek inexplicably appears to chide Sanyo for including an explicit claim limitation as part of the claim construction. MediaTek asks the Court to strike from the claim the clause which states, "thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function." (MT Ex. A at 20:29-32). However, MediaTek relies upon inapposite case law for this request. In the case cited by MediaTek, the Court stated, "a whereby clause that merely states

[6] MT Ex. D at pp. 3-4.

the result of the limitations in the claim adds nothing to the substance of the claim." *Lockheed Martin*, 324 F.3d at 1319. There is no showing that the "thereby" clause of claim 11 adds nothing to the substance of the claim. Neither the patentees nor MediaTek made any showing that all existing conversion equations have the "symmetrical relation . . . derived from the cosine function" properties. Rather, the patentees claimed that one of the equations in the patent (i.e., equation (6)) has symmetrical properties without making such claims about other equations in the patent or in the art. (MT Ex. A at 15:60 - 16:15). Thus, because there is no showing that all conversion equations have the "symmetrical" properties, the recited function (both before and after the term "thereby") is a necessary part of the construction of this limitation. Accordingly, Sanyo respectfully requests that the Court identify the entire claimed function when construing this claim; otherwise, an improper corresponding structure may be associated with the function. Sanyo requests that the Court construe the function in claim 11 as:

"converting frequency domain audio data from the frequency domain to a time domain using a symmetrical cosine function with respect to each of multiple channels of audio data, resulting in two sets of time domain audio data that are symmetrical by nature."

Regarding the function in claims 13 and 16, MediaTek merely reiterates the claim language without proposing an ordinary meaning of the terms. Sanyo proposes ordinary meanings of the terms which remain true to the claim language and will be better understood by a jury. Sanyo requests that the Court construe the function in claims 13 and 16 as:

"converting each of the multiple channels of frequency domain audio data from frequency domain audio data to time domain audio data."

Structure

The single statement of structure proposed by MediaTek, for all of the claims, lacks the required specificity. "A means-plus-function claim encompasses all structure in the

specification corresponding to that element and equivalent structures." *Micro Chem.*, 194 F.3d at 1258. MediaTek identifies specific structure from the specification that it associates with the claimed function. (MT Br. 16). However, MediaTek then requests that the Court identify a generic "frequency base to time base converting circuit" or an "inverse MDCT circuit" as the required structure. (*Id.* at 17).

MediaTek's request that the Court include "frequency base to time base converting circuit or inverse MDCT circuit" in its identification of structure is a distinction without distinction. (MT Br. 17). Both are the same. (MT Ex. A at 4:60-61 states "IMDCT circuit (frequency base to time base converting circuit) 33"). Accordingly, Sanyo does not dispute that both circuits can be identified as corresponding structure, provided that the construction also identifies the appropriate equation(s) implemented by the circuits.

Sanyo respectfully requests that the Court identify specific down mixing structure from the specification, as proposed by Sanyo. The '819 patent specifically identifies the equation to use for the conversion. It states, "A frequency base to time base converting process which is executed by the IMDCT circuit 33 is described by the following equation (2)." (MT Ex. A at 3:43-45). Figures 9, 12, 14, 15, and 16 all show an "IMDCT circuit," the circuit that is associated with equation (2), instead of a generic converting means. (*Id*. at 3:43-45, Figs. 9, 12, 14, 15, 16).

In the '819 patent, equation (2) is the same as equation (5). (MT Ex. A, *compare* 3:46-57 *to* 15:47-60). The patent introduces equation (6) as a derivation of equation (5). (*Id*. at 15:60-16:12). Equation (6) is employed in certain embodiments of the purported invention, *e.g.* claim 11. The '819 patent describes using equation (6) to derive one portion of a set of values (called k=N/4~N/2-1) from an original set of values (called k=0~N/4-1). (*Id*. at 15:60-16:15).

Using this equation, a second set of data can be derived from a first set of data, when the data sets have symmetry as is required by the language of claim 11. (*Id.*).

Equation (7) is used for conversion when half of the data to be converted is delayed. (MT Ex. A at 16:15-16). This equation does not appear to relate to any of the claims.

Other than the enumerated equations (2), (5), (6), and (7), the '819 patent does not set forth any equations for use in converting data from the frequency domain to the time domain. "[T]he corresponding structure for a § 112 ¶ 6 claim for a computer-implemented function is the algorithm disclosed in the specification." *Harris Corp.*, 417 F.3d at 1249. Thus, for claims 1, 3, 13, and 16, Sanyo respectfully requests that the Court identify equation (2) as part of the corresponding structure for all of those claims. Because claim 11 is directed to "frequency base to time base converting means" wherein "a first and a second set of time domain audio data hav[e] a symmetrical relation to each other derived from [the] cosine function," Sanyo respectfully requests that the Court identify equations (5) and (6) as part of the corresponding structure for claim 11.

Sanyo proposes that the structures be identified as follows:

for claims 1, 3, 13, and 16: "an IMDCT circuit implementing equation (2)," and for claim 11: "an IMDCT circuit implementing equations (5) and (6)."

3. Separating Means (Claim 3)

Function

The parties agree as to the identified function of the separating means.

Structure

The structure proposed by MediaTek is disputed because it lacks the required specificity. *See Micro Chem.*, 194 F.3d at 1258. Nowhere does MediaTek identify specific

structure from the specification. Instead, MediaTek requests that the Court identify a generic "demultiplexing circuit" and "buffer memory" as the required structure. (MT Br. 18).

The Court should identify specific down mixing structure from the specification, as proposed by Sanyo. The '819 patent specifically notes that "the separating process . . . of the multiplexed data [is performed] in the DMUX 1." (MT Ex. A at 12:42-45; *see also* 11:32-42). The patent equates element 31 with the DMUX 1. (*Id.* at 11:32-38). It also notes "In FIG. 7, encoded data . . . is separated . . . by the demultiplexing circuit 31." (*Id.* at 8:32-36). Sanyo requests that the Court conclude find that "a demultiplexing circuit as shown in element 31 of Fig. 7, or a demultiplexing circuit included with an inverse quantizing circuit as shown in element 1 of Fig. 9," which were purposefully included in the patentees' description of the purported invention, correspond to the identified function.

The identified function of the "separating means" does not include storage of the separated data in memory. It is improper to "incorporat[e] ... structure from the written description beyond that necessary to perform the claimed function." *See Micro Chem.*, 194 F.3d at 1258; *see also* MT Br. 23. Accordingly, MediaTek's proposal to include "separately or in combination with a buffer memory" in the proposed structure is inappropriate as a matter of law.

4. Down Mixing Means (Claims 13 and 16)

Function

Again, MediaTek reiterates the claim language. Sanyo has again proposed ordinary meanings of the terms that remain true to the claim language and will be better understood by a jury. Accordingly, Sanyo respectfully requests that the Court adopt the following construction of the functions:

for claim 13, "processing the time domain audio data and mixing multiple channels of time domain audio data into a predetermined number of channels at a predetermined

level ratio by adding down mixed time domain audio data stored in the PCM 'buffer memory' to the time domain audio data output from the 'window applying means;' then storing the down mixed time domain audio data in the same PCM 'buffer memory,'"

and for claim 16, "mixing multiple channels of time domain audio data into a predetermined number of channels at a predetermined level ratio by adding delayed data stored in the delay buffer from the window applying means to time domain audio data output from the window applying means; then storing the down mixed time domain audio data in the delay buffer memory."

Structure

The structure proposed by MediaTek is disputed because it lacks the required specificity. *See Micro Chem.*, 194 F.3d at 1258. Nowhere does MediaTek identify specific structure from the specification. Instead, MediaTek requests that the Court identify a generic "down mixing circuit" as the required structure. (MT Br. 24).

Sanyo contends that the structure should be construed as a down mixing circuit implementing equation (3). The functions identified for claims 13 and 16 include "a predetermined level ratio." A generic down mixing means may not require a predetermined level ratio. For example, the ratio may be uneven rather than level or may be adjusted during processing rather than predetermined. However, where the identified function calls for a "predetermined level ratio," the law requires identification of structure that implements "a predetermined level ratio." The only structure identified by the '819 patent for implementing this ratio in a "time domain" down mixer is a circuit implementing equation (3). (MT Ex. A at 4:33-40).

As already explained in the discussion of "frequency domain down mixing means," equation (4) is the mathematical form of the process implemented by the frequency

domain down mixing means. "[T]he corresponding structure for a § 112 ¶ 6 claim for a computer-implemented function is the algorithm disclosed in the specification." *Harris Corp.*, 417 F.3d at 1249.

The same analysis applies here. Comparison of equations (3) and (4) shows that the equations are virtually identical. (*Id*., *compare* 4:20-32 *to* 9:12-27). The only difference is that equation (4) is defined as handling frequency domain signals (*Id.* at 9:21-23), while equation (3) is defined as handling time domain signals. (*Id.* at 4:37-40, Fig. 4). This is the same difference between the previously discussed "frequency domain down mixing means" and the "down mixing means" now being discussed. (*Id*., *compare* 4:22-32 *to* 9:16-27). Thus, a circuit that implements equation (3) is part of the corresponding structure.

Accordingly, Sanyo respectfully requests that the Court adopt the structure set forth by Sanyo.

B. The '486 Patent

The parties presently dispute the constructions for four claim terms in the '486 patent, none of which are means-plus-function terms.[7]

1. Fixed Frequency (All Asserted Claims)

All asserted claims of the '486 patent include the "fixed frequency" limitation that appears in the context of "fixed frequency horizontal deflection signal."[8]

Based on its ordinary meaning and the intrinsic evidence, "fixed frequency" should be construed as "a frequency that cannot be changed."

[7] Sanyo no longer disputes MediaTek's construction of the terms "display format" and "system clock signal."

[8] These include independent claims 1-2 and dependent claims 6 and 8-11.

Latching on to a lone sentence in the specification that uses the word "single" to describe the horizontal scanning frequency of the display device and completely ignoring the teachings of the claims and the specification, MediaTek proposes that "fixed frequency" means "single frequency."

MediaTek attempts to rewrite the claims by asserting that claim 1 shows "a fixed frequency horizontal deflection signal" being "generated in response to a raster clock signal," thereby indicating that the frequency changes with the input signal. (MT Br. 26). Claim 1, however, does not support such a reading. Claim 1 talks about the frequencies of *both* the horizontal and the vertical deflection signals:

> Apparatus for processing an input video signal having one of a plurality of display formats to produce an output video signal suitable for use by a display device, said display device utilizing a ***fixed frequency horizontal deflection signal and a vertical deflection signal***, said apparatus comprising:
>
> ... a raster generator, for generating, in response to a raster clock signal, said ***fixed frequency horizontal deflection signal*** and said vertical deflection signal, said ***vertical deflection signal having a frequency defined by*** a vertical display format of said ***output video signal*** ...

When describing the frequency of the horizontal deflection signal, the claim uses the word "fixed." On the other hand, when describing the frequency of the vertical deflection signal, the claim uses the words "a frequency defined by ... output video signal." This implies that the frequency of the vertical deflection signal *changes* based on the output video signal, i.e., the frequency is not fixed. If the inventor wanted to claim a horizontal deflection signal whose frequency changes based on the input video signal, the inventor easily could have used similar language. For example, the inventor could have said "horizontal deflection signal having a frequency defined by a input video signal." But the inventor did not. The fact that the word "fixed" is used confirms that the inventor wanted to draw a distinction between the frequencies

of the two deflection signals – the horizontal is fixed while the vertical is not.[9] Therefore, the word "fixed" implies that the frequency of the horizontal deflection signal does not change.

Moreover, according to the principles of statutory construction, each word in a claim must have a meaning. Here, the word "fixed" in claim 1 must have a meaning. But if "fixed" means "single," as proposed by MediaTek, it makes no sense because "a single frequency" simply means "a frequency." Therefore, MediaTek's construction for the word "fixed" effectively removes that limitation from the term "a fixed frequency."

That the horizontal deflection frequency does not change based on the raster clock is also confirmed by dependent claim 9. Claim 9 provides that the raster clock can be 67.5, 81, 94.5 or 108 MHz. Reading it in the context of independent claim 1, this means that each of the four values of the raster clock generate the *same* "*said fixed frequency"* horizontal deflection signal.

Moreover, to the extent MediaTek equates "scanning" frequency to "deflection" frequency, claim 2 is also instructive. (*See* MT Br. 25). Claim 2 is directed to a display device having a "substantially fixed horizontal scanning frequency" or "substantially fixed frequency horizontal synchronizing signal." If as MediaTek proposes, fixed frequency means the use of a single frequency over a period of time, the limitation in claim 2 makes no sense. A signal can have a single frequency or it can have multiple frequencies. It cannot be substantially single. On the other hand, it can be "substantially fixed," where slight variations off of the fixed frequency are permitted. "Generally, a term should be given the same meaning throughout the patent."

[9] This is consistent with the way the two deflection signals are described in the specification: "generating in response to the raster clock signal, a fixed frequency horizontal synchronizing signal and a vertical synchronizing signal." (MT Ex. B at 2:61-63; s*ee also*, 6:40-43; 51-57).

Good Sportsman Mktg. LLC v. *Testa Assocs., LLC*, No. 6:05-cv-90, slip op. at 14-15 (E.D. Tex., July 12, 2006).

Any remaining question is conclusively resolved by looking at the specification. The specification explains that the horizontal deflection signal has the same frequency *regardless* of the raster clock:

- Raster generator 190 generates a ***fixed frequency horizontal deflection signal*** H-DEF and a vertical deflection signal V-DEF in a conventional manner in response to a raster clock signal f_{RAST}. .... For example, a *horizontal deflection signal H-DEF* ***having a frequency of 33.75 kHz may be generated by dividing, e.g., a 67.5 MHz raster clock f_{RAST} by 2000, or by dividing an 81 MHz raster clock f_{RAST} by 2400***. (MT Ex. B at 6:40-55).
- The information contained within Table 2 is directed toward a ***display device having a fixed horizontal deflection frequency of 33.75 kHz***, and a total of 1125 lines (including active and blanking lines) ... In the first example includes the raster clock frequency ***f_{RAST} is 67.5 MHz, while in the second example the raster clock frequency is 81 MHz***. (*Id*. at 10:37-56).

As with its erroneous assertion that fixed frequency changes with the raster clock, MediaTek's assertion that the horizontal deflection frequency changes because it is "separately derived for each new input video stream" is also completely unsupported. (MT Br. 26). In distinguishing his invention over prior art during prosecution, the applicant clearly disavowed that the frequency of the horizontal deflection signal changes with the input video signal:

> The [Hirohata television] receiver ***adapts*** both the horizontal and vertical scanning frequencies of the display device ***to whichever signal is received***. ***This is not at all like the subject invention, which utilizes a fixed horizontal scanning frequency*** and adapts a vertical scanning frequency in response to a display format of an input video signal. (Ex. 3) (first underlined emphasis in original).[10]

Accordingly, MediaTek is estopped from arguing that the frequency of the horizontal deflection frequency changes with the input signal. *Sextant Avionique* v. *Analog*

[10] Given this unequivocal statement, it is not surprising that MediaTek completely ignores it. While MediaTek states that claims must be construed by focusing on the prosecution history, MediaTek nevertheless fails to follow it. In fact, no where in the forty five pages of its brief is there any discussion of any prosecution history of any of the patents-in-suit.

Devices, Inc., 172 F.3d 817, 828 n.3 (Fed. Cir. 1999) (prosecution history estoppel arises not only from claim amendments, but also from arguments submitted to obtain the patent, whether or not actually required to secure allowance of a claim).

Indeed, the very reason to keep the horizontal deflection frequency unchanged in the claimed invention is to make the circuitry cheaper and avoid the problems that occur when the horizontal deflection frequency changes with the input signal:

- ***It is known*** in the computer industry to display multiple graphics formats on a so-called "multisync" display device. Specifically, a ***multisync display changes horizontal*** and/or vertical ***scanning frequencies in response to a change in graphics format*** ... ***Unfortunately, the multisync approach leads to an increase in cost*** due to the more complicated deflection circuitry, an increase in power consumption, and a high inter-format switching latency ... (MT Ex. B at 1:46-60).
- Thus, the Hirohata patent utilizes an ***old method*** (such as noted in the background of the subject application) o***f adapting horizontal deflection frequencies in response to changes in input video signals***. This method ***disadvantageously*** produces annoying visual artifacts and format switching latency. (Ex. 3 at 10).
- ***To further reduce system cost***, the DTV receiver 100 of FIG. 1 ***provides a fixed horizontal scanning frequency*** for use by the display device 175. (MT Ex. B at 8:64-66).

Finally, Sanyo's proposed construction conforms with the ordinary meaning of the word "fixed" which is "[n]ot subject to change or variation; constant." *See* American Heritage College Dictionary (3d ed. 1997) (Ex. 4). *Phillips*, 415 F.3d at 1322-23 (courts may rely on dictionary definitions "'so long as the dictionary definition does not contradict any definition in or ascertained by a reading of the patent documents.'") (citation omitted).

Therefore, consistent with its ordinary meaning and the intrinsic evidence, "fixed frequency" should be construed as "a frequency that cannot be changed."

2. Raster Clock Signal (All Asserted Claims)

Consistent with the intrinsic evidence, "raster clock signal" should be construed as "a signal with a nonstandard frequency easily derived in response to a program clock reference (PCR)."

MediaTek baldly asserts that the ordinary meaning, the claims and the specification all require that the term be construed as "a periodic signal used to synchronize a display device." But neither the claim language nor the specification (4:45-49) that MediaTek cites as support for its construction even have the words "periodic" or "synchronize" or their synonyms. Moreover, MediaTek's alleged ordinary meaning of this limitation completely ignores the specification.

The ordinary meaning of a term is controlling only where the inventor has not acted as his own lexicographer. *Philips*, 415 F.3d at 1316 (where the specification reveals "a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess," or reveals the "correct claim scope" dictated by the inventor, the "inventor's lexicography governs").

Here the specification unambiguously reveals that the inventor acted as his own lexicographer and provided a special meaning to the term "raster clock signal." According to the inventor, the claimed raster clock signal has two features – it is generated in response to a PCR and has a non-standard frequency that is easily derived. Therefore, even assuming that MediaTek is correct on the ordinary meaning of the term "raster clock signal," which it is not, that meaning cannot stand.

The intrinsic evidence leaves no doubt that the raster clock signal is defined as being generated from the PCR. To begin with, the language of the claim itself makes it clear that the raster clock signal is generated in response to the PCR: "a method for generating video and

timing signals ... comprising the steps of ... ***generating, in response to a program clock reference (PCR)*** associated with said video stream, a system clock signal and ***a raster clock signal***." (Claim 2). MediaTek does not dispute that this claim language requires that raster clock signal be generated in response to the PCR. Rather, MediaTek asserts that construing raster clock signal to include this requirement in light of the claim language somehow makes that language redundant. (MT Br. 27).

Under MediaTek's logic, the only use for the claim language is to show what cannot be a part of the construction. That is not the law. The Federal Circuit has made it clear that it is entirely appropriate, in fact it is required, that terms be construed by looking at the language of the claims. *Philips*, 415 F.3d at 1324 (holding that the claim language "'further means disposed inside the shell for increasing its *load bearing capacity* comprising internal *steel* baffles extending *inwardly* from the steel shell walls'" imposes three requirements for "baffles" – that they be made of steel, be part of load-bearing means for the wall section, and be pointed inward from the wall section). Further, the *Philips* court explained that a claim term cannot be construed to include a limitation that is expressly present in the language of *another claim. Id*. at 1324-25.

The specification and the prosecution history further confirm that the raster clock signal is defined to be generated from the clock reference PCR:

- ***The invention provides*** a multiple format video signal processing system operating in conjunction with a display device timing system ... the display device timing system comprises a clock circuit that produces a system clock and ***raster clock signal that are easily derived from a transport stream clock reference***. (summary of the invention at MT Ex. B, 2:22-32).
- A method for generating video and timing signals ***according to the invention***, ... comprises the steps of receiving the video stream and an associated format indicia; ***generating, in response to a reference clock signal associated with the video stream, a raster clock signal***. (summary of the invention at MT Ex. B, 2:54-61).

- To distinguish Yoshida patent, "[a]pplicants have ***amended both independent claims to clearly indicate that*** the clock circuit of claim 11 and the step of generating a system clock signal and ***a raster clock signal of claim 12 are responsive to a program clock reference (PCR)*** that is associated with the input video signal being processed. (Ex. 5 at 6).
- The Arai arrangement also clearly fails to ***utilize a program clock reference to generate a system clock and a raster clock, as claimed in the subject invention.*** (Ex. 5 at 8).
- Applicant argues that neither references of Arai and Yoshida discuss that ***PCR program clock reference is utilized to generate a system clock and a raster clock***, where the PCR is a 27 MHz clock signal. (Ex. 6).

To secure allowance of claims, applicant amended the claims to add the limitation of raster clock signal being generated *in response to PCR*. Applicant thus narrowed the scope of the claimed raster clock so that it was not just any raster clock, but a raster clock generated in response to the PCR. MediaTek is now estopped from seeking the broader construction. *Sextant Avionique*, 172 F.3d at 828 n.3.

The intrinsic evidence also unambiguously shows that the inventor defined the raster clock signal to have a non-standard frequency that is easily derived. Contrary to MediaTek's assertion, the non-standard frequency limitation is not just in the preferred embodiment but is the essence of the claimed invention. In fact, the non-standard frequency of the raster clock is an alleged novel feature of the invention. The "summary of the invention" states:

> ***Part of the invention lies in the recognition*** by the inventor that display ***raster signals do not need to conform to the waveforms commonly used*** in prior art display driver circuits, studio equipment and production standards. Specifically, the inventor recognized that considerable cost savings may be achieved in a multiple video format system ***by utilizing a raster (pixel) clock*** and horizontal and vertical deflection frequencies ***that are easily derived*** from the 27 MHz system clock ... (MT Ex. B at 2:33-42).

Moreover, *after* describing the preferred embodiment, the specification explicitly lists the criteria for choosing raster clock frequencies *other* than those used in the preferred embodiment – the frequencies should be easy to derive and not be standard:

> It must be noted that the ***invention contemplates the use of*** other native display formats and ***other raster frequencies. The criteria*** for adapting the various DTV formats for display on different display devices ***is detailed above***. First, a raster frequency f_{RAST} ***is selected that is both easy to scale*** from the system clock (e.g., 27 MHz for MPEG systems), a***nd near the conventional display clock frequency*** for the particular type of display device selected. (MT Ex. B at 13:7-14).

Thus, the entire specification consistently explains that the raster clock signal must have a non-standard frequency and must be easily derived from the system clock signal. These two aspects are related. The raster clock is easily derived from the 27 MHz system clock because it has a non-standard frequency. No where in the specification is there any teaching of how to generate a raster clock having the standard frequency of 74.25 MHz using the system clock. All the examples disclosed are of raster clocks having frequencies other than 74.25 – 67.5 MHz, 81 MHz, 94.5 MHz, or 108 MHz. (MT Ex. B at 4:45-51; 8:13-25; 9:21-34). Indeed, the specification touts the advantage of using non-standard raster clock frequencies. Hence, construing the raster clock signal to have any frequency would effectively eviscerate the purpose of the invention. *Howmedica Osteonics Corp*., 401 F.3d at 1372-73 (adopting a two-dimensional measurement for "transverse sectional dimensions" because a one-dimensional measurement "would defeat the purpose of the invention to provide a snug fit").

Accordingly, contrary to MediaTek's assertion, the non-standard aspect of the raster clock signal is not a limitation of the preferred embodiment, but an essential part of the invention itself. *SciMed Life Sys*. v. *Advanced Cardiovascular Sys*., 242 F.3d 1337, 1341 (Fed. Cir. 2001) ("Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question."); *Wang Labs, Inc*. v. *Am. Online, Inc.*, 197 F.3d

1377, 1383 (Fed. Cir. 1999) (when the "preferred embodiment" is described as the invention itself, the claims are not entitled to a broader scope than that embodiment).

Construing raster clock signal to have a nonstandard frequency that is easily derived is also consistent with dependent claims 9 and 18 that provide four examples of such non-standard raster frequencies (67.5, 81, 94.5, 108), all of which are easily derived from the 27 MHz system clock.

Therefore, consistent with the intrinsic evidence and the purpose of the invention, "raster clock signal" should be construed to mean "a signal with a nonstandard frequency easily derived in response to a program clock reference (PCR)."

3. Clock Circuit (Claims 1, 6 and 8-10)

Independent claim 1, and dependent claims 6 and 8-10 include the "clock circuit" limitation.

Solely based on a dictionary definition, MediaTek proposes that this term be construed to mean "a collection of electrical elements for producing clock signals." This proposal is puzzling given MediaTek's correct statement that in claim construction, "extrinsic evidence – particularly dictionary definitions – should be employed sparingly and only to conform the meaning of the intrinsic evidence." MediaTek, however, fails to follow that standard. (MT Br. 12).

The law is clear that we look to the specification of the patent first to determine the meaning of a claim term. *Philips*, 415 F.3d at 1313 ("[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.").

Consistent with the intrinsic evidence and the purpose of the invention, Sanyo contends that "clock circuit" should be construed to mean "a circuit using a single voltage

controlled oscillator (VCO), that reacts to a program clock reference (PCR) of the input video signal to generate both the system clock and the raster clock."

The intrinsic evidence makes it plain that the claimed clock circuit is not any clock circuit but a specific clock circuit having three features – a single VCO, it responds to the PCR, and it generates both the system and raster clocks.

The language of the claim itself makes it clear that the clock circuit generates both the system and raster clocks in response to the PCR: "a ***clock circuit, responsive to a program clock reference (PCR)*** associated with said input video signal, ***for producing a system clock signal and said raster clock signal***." (Claim 1). As with the construction for "raster clock signal," MediaTek asserts that this claim language can only be used to show what a "clock circuit" does not encompass. (MT Br. 29). MediaTek is, once again, wrong.

Under MediaTek's logic, a term can never be construed to include a limitation that explicitly appears in the same claim itself. That makes no sense. As Sanyo explained in the section dealing with the "raster clock signal," a term must be construed in light of the claim language. A claim term can be construed to exclude a limitation dictated by the claim itself when the specification or the prosecution history or another claim is inconsistent with that limitation. *See Philips*, 415 F.3d at 1316, 1324-25. That is not the case here.

The specification and the prosecution history overwhelmingly and consistently support that the clock circuit generates both the system and raster clocks in response to the PCR:

- ***The invention provides*** a multiple format video signal processing system operating in conjunction with a display device timing system ... the display device timing system comprises ***a clock circuit that produces a system clock and raster clock signal*** that are easily derived ***from a transport stream clock reference***. (summary of the invention at MT Ex. B, 2:22-32).
- ***The invention*** is an apparatus ... the apparatus ***comprising: a clock circuit, for producing a first clock signal*** suitable for deriving all necessary clock signals used within at least a

decoder portion of the system, and ***suitable for use as a display [raster] clock***, including ***a second clock signal suitable for use as a system clock***. (MT Ex. B at 3:10-14).

- The only embodiment of Figure 1 shows a clock circuit 110 that uses the PCR as an input and generates both the system clock f_{SYS} and the raster clock f_{RAST}. (*Id*. at Fig. 1; *see also* 4:38-46).
- To distinguish Yoshida patent, "[a]pplicants have ***amended both independent claims to clearly indicate that*** the clock circuit of claim 11 and the step of ***generating a system clock signal and a raster clock signal of claim 12 are responsive to a program clock reference (PCR)*** that is associated with the input video signal being processed. (Ex. 5 at 6).
- The Arai arrangement also clearly fails to ***utilize a program clock reference to generate a system clock and a raster clock, as claimed in the subject invention.*** (Ex. 5 at 8; *see also* Ex. 6).

The intrinsic evidence also shows that the clock circuit has a single voltage controlled oscillator VCO. The VCO is the principal component of the clock circuit that generates a clock of a given frequency:

- One ***advantage of*** the above-described ***invention*** allows the use of a ***single precision clock source***, such as a voltage controlled crystal oscillator, ***to derive all necessary clock signals***. (MT Ex. B at 13:1-3).
- The above-described ***invention advantageously provides*** for a DTV receiver having a ***single master clock [i.e., VCO] producing a raster or pixel clock from which a 27 MHz system clock*** and, optionally, an additional decoder clock having a different frequency is easily ***synthesized***. (*Id*. at 13:60-64).
- The only embodiment of Figure 1 shows a single clock circuit 110 that has a single VCO 114 that generates both the system clock f_{SYS} and the raster clock f_{RAST}. (*Id*. at Fig. 1; *see also* 4:55-64).

Thus, contrary to MediaTek's assertion, use of single VCO is not just a limitation present in the preferred embodiment, but a limitation of the invention itself. In fact, this was the reason the inventor was able to make the circuitry simpler – rather than use different clock circuits to generate different clocks (which was what was done in the prior art), use the same clock circuit to generate all clocks. Indeed, any broader construction of "clock circuit" without the single VCO limitation would eviscerate the purpose of the invention. *Howmedica Osteonics Corp*., 401 F.3d at 1372-73.

Further, MediaTek's assertion that presence of the word "comprises" in the specification somehow allows the claimed clock circuit to have more than one VCO is entirely misplaced. (MT Br. 29). The fact that the specification uses the word "comprising" when describing a claimed component is irrelevant unless the word comprising is used with that element, and that is not the case here. Here, while claim 1 does contain the word "comprising," it is used in the preamble – not in the "clock circuit" limitation. Therefore, "comprises" in the claim may allow for additional components in the processing apparatus (besides the recited components of "format converter," "frame rate converter," "raster generator," and "clock circuit"), but not additional elements within each component. *Invitrogen Corp*. v. *Biocrest Mfg*., 327 F.3d 1364, 1368 (Fed. Cir. 2003), the case that MediaTek relies on, is inapposite. *Invitrogen Corp.* addresses the affect of the word "comprising" when present in the *claim*, not specification – "[T]he transition 'comprising' in a method claim indicates that the claim is open-ended and allows for additional steps." *Id*. In fact, *Invitrogen Corp.* implies that the absence of the term "comprises" from the "clock circuit" component means that the term cannot be construed to allow for additional elements.

Furthermore, Sanyo's proposed construction also conforms with the extrinsic evidence. A circuit is defined as "the complete path of wires and equipment along which an electric current flows." *See* Oxford Advanced Learner's Dictionary (4th ed. 1989) (Ex. 7). *See Phillips*, 415 F.3d at 1322-23. As illustrated in Figure 1, the clock circuit 110 having a VCO outputs the system and raster clocks in response to the PCR input and represents a *complete path* along which current flows.

Accordingly, consistent with the intrinsic evidence, the purpose of the invention, and the extrinsic evidence, "clock circuit" should be construed as "a circuit using a single voltage

controlled oscillator (VCO), that reacts to a program clock reference (PCR) of the input video signal to generate both the system clock and the raster clock."

4. Frequency Scaling (All Asserted Claims)

All asserted claims of the '486 patent include the "frequency scaling" limitation that appears in the context of "said raster clock signal being generated by frequency scaling said system clock."

Based on the description of a specific embodiment and ignoring the teachings of the specification and the purpose of the invention, MediaTek proposes to construe this term to mean "multiplying or dividing a frequency by a given factor." The only intrinsic evidence that MediaTek cites as support for its construction is a single sentence from the description of the preferred embodiment of Figure 1. (MT Ex. B at 4:57-67). But, contrary to MediaTek's assertion, a person of ordinary skill in the art would not understand the scaling taught in the patent to be *any* multiplication or division because he would understand scaling *in the context* of the specification, not in a vacuum. *Phillips*, 415 F.3d at 1313.

Consistent with the intrinsic evidence and the purpose of the invention, "frequency scaling" should be construed as "doubling and/or dividing a given frequency by easily derived values to obtain a different frequency."

While the claim language itself does not throw any light on how the frequency should be scaled, a review of the specification makes it abundantly clear that what is taught by the patent is generating the raster clock frequency by easy or simple scaling. The only thing the patent teaches is generating the raster clock as a simple ratio of the system clock, e.g., 81 MHz raster clock and 27 MHz system clock – use a divider circuit (divide 81 by 3 to get 27).

It is well known that a circuit that performs a division operation is a relatively simple circuit. Doubling a frequency may also be achieved by using a simple circuit. But a

circuit that performs multiplication by a factor greater than two is a complex circuit that typically requires a VCO. Every single example disclosed in the specification is consistent with using a simple circuit. For example, the specification refers to the use of both 67.5 MHz and 94.5 MHz as raster clock frequencies. A 67.5 MHz raster clock can be easily scaled to 27 MHz – divide by five followed by doubling to get 27 MHz. (MT Ex. B at 4: 60-64). Similarly, a 94.5 MHz raster clock can be easily scaled to a 27 MHz system clock in a 7:2 ratio – divide by 7 followed by doubling. (*Id*. at 9:27-31). The patent denotes these ratios as "94.25 MHz (7x27 MHz/2)" – this does not mean that you multiply by 7 followed by divide by 2. (*Id*.). Indeed, the only way to generate 94.25 MHz and 27 MHz clocks, using a single VCO as the patent teaches, is to divide 94.25 MHz by 7 and then double it to obtain 27 MHz. (3:10-14). There is no teaching whatsoever of generating a 74.25 MHz clock and 27 MHz system clock which would require relatively complex circuitry – divide 74.25 by 11 and then multiply by 4. Indeed, there is no teaching of performing any multiplication greater than two. As explained in the construction for "raster clock signal," the patent, in fact, teaches away from using 74.25 MHz raster frequency.

Moreover, the specification confirms that the requirement that scaling be done by easily derived values is not just in the disclosed examples, but in the invention itself:

- As previously mentioned, ***an aspect of the present invention is the utilization of raster clock frequencies*** f_{RAST} and horizontal deflection frequencies H-DEF ***that are related in a straightforward manner to the 27 MHz system clock*** $f_{SYS.}$ A typical raster clock frequency that is used for both 1920x1080 and 1280x720 format video signals is 75 MHz. As such, several of the raster clock frequencies f_{RAST} deemed by the inventor to be useful in practicing the invention are 67.5 MHz (5x 27 MHz /2) [5:2 ratio], 81 MHz (3x 27 MHz) [3:1 ratio], 94.5 MHz (7x 27 MHz/2) [7:2 ratio] and 108 MHz (7x27 MHz) [*sic,* 4:1 ratio]. As previously discussed with respect to timing circuit 110, ***these raster clock frequencies*** f_{RAST} ***are relatively easy to produce*** using various known frequency scaling techniques. (MT Ex. B at 9:21-34).
- Moreover, the ***raster frequencies*** of 67.5 MHz and 81 MHz ***in the exemplary embodiment may be adapted*** to be similar to a raster frequency native ***to the different display device***. Specifically, a raster clock f_{RAST} ***may be selected that is easily derived***

from a system clock, yet similar to the raster frequency typically used in a the different display device. (*Id*. at 12:46-52).

- ***The criteria*** for adapting the various DTV formats for display on different display devices ***is detailed above***. First, a raster frequency f_{RAST} ***is selected that is both easy to scale*** from the system clock (e.g., 27 MHz for MPEG systems) ... (*Id*. at 13:7-14).
- Thus, the above described 67.5 MHz and 81 MHz frequencies ***are attractive since*** they are both near 74.25 MHz, and they ***are both easily derived from the 27 MHz system clock*** $f_{SYS.}$ (*Id*. at 8:18-21).

Further, as with the non-standard frequency feature, using simple scaling is the means of achieving the stated goal of making the circuitry simpler and cheaper:

- Specifically, ***the inventor recognized that considerable cost savings may be achieved*** in a multiple video format system ***by utilizing a raster (pixel) clock*** and horizontal and vertical deflection frequencies ***that are easily derived from the 27 MHz system clock*** used for receiver synchronization in an MPEG-like video processing system. (summary of the invention, MT Ex. B at 2:37-342).
- Moreover, ***by selecting a raster frequency that is easily derived from the system clock*** the ***scaling circuitry*** necessary to produce the raster clock ***is greatly simplified***. (*Id*. at 12: 60-63).

Thus, construing that frequency scaling be done by using easily derived values is mandated by the specification and is a limitation of the invention itself, not just the preferred embodiment. *SciMed Life Sys*., 242 F.3d at 1341.

Consistent with the intrinsic evidence and the purpose of the invention, "frequency scaling" must be construed as "doubling and/or dividing a given frequency by easily derived values to obtain a different frequency."

C. The '356 Patent

While the parties had previously disputed the constructions for eight claim terms in the '356 patent (six of which are means-plus-function terms), Sanyo no longer disputes MediaTek's revised proposed constructions for three of these terms.[11]

[11] The terms are "control means," "a first control means," and "encoding information." The parties agree that "control means" and "a first control means" are means-plus-function limitations that must be construed pursuant to 35 U.S.C. § 112(6).

The parties agree that the first four disputed terms to be construed for the '356 patent are "means plus function" limitations that must be construed pursuant to 35 U.S.C. § 112(6). (MT Ex. D at 15).

1. Video encoding means (Claims 1 and 7)

The parties agree that this limitation is a means plus function limitation. Sanyo and MediaTek, however, disagree on the proper construction for this term in virtually every other respect. This includes the identification of what the claimed function is.

Function

MediaTek improperly attempts to limit the claimed function to "encoding a video signal into video data"

Sanyo's proposed construction of the function of this term includes:

"*Encoding* a video signal into video data, *attaching* encoding information to said video data to generate encoded video data, *and generating* data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit."

Sanyo's proposed construction is fully supported by the language of the claim itself, which includes three distinct functions for this element: "encoding," "attaching" and "generating." *See Micro Chem.*, 194 F.3d at 1257-58. Moreover, the specification clearly sets forth each of these three sub-functions: "The encoder circuit 11 creates encoded video data from the received video signal," (MT Ex. C at 3:52-54); "The multiplexer circuit 13 attaches the GOP, sequence and picture headers to the GOP and respective picture data to create an encoded bit stream based on the MPEG2 standard," (*Id.* at 4:14-17); "The header circuit 12 also determines a length of the bit stream, e.g., between the picture headers, that is, a bit length L." (*Id.* at 4:20-22).

Structure

MediaTek's proposed structure for this means element does not support the proper construction of the function, because MediaTek correlates the structure with encoder circuit 11. Moreover, MediaTek's proposed construction is directly at odds with the disclosed "means for encoding a video signal" of the '356 patent. (MT Ex. C at 3:49-51).

The specification of the '356 patent clearly describes that the encoder circuit 11 is merely one component of the video signal encoder that operates as the properly construed structure for this means-plus-function element:

"The video signal encoder 1, ***which constitutes a means for encoding a video signal***, includes an encoder circuit 11, a header creation circuit 12 and a multiplexer circuit 13." (MT Ex. C at 3:49-51).

The '356 patent also explains the algorithm by which the encoder circuit 11 operates, stating, "The encoder circuit 11 creates encoded video data . . . on the basis of an encoding rule such as an MPEG1 or MPEG2 standard." (MT Ex. C at 3:53-55). The multiplexer circuit 13 "create[s] an encoded bit stream based on the MPEG2 standard." (*Id.* at 4:14-19). Thus, the algorithms to apply the MPEG1 or MPEG2 standards are part and parcel of the corresponding structure identified in the '356 patent. *See WMS Gaming, Inc*., 184 F.3d at 1349 ("In a means-plus-function claim in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm.").

It matters not that the patentee called this structure an "embodiment" or "example." For purposes of construing the claim under 35 U.S.C. § 112(6), this structure is the only "video encoding means" structure in the specification that is capable of performing the

claimed function. "Section 112 ... permits means-plus-function language in a combination claim, but with a 'string attached.' The 'attached string' limits the applicant to the structure, material, or acts in the specification and their equivalents." *Valmont Indus., Inc. v. Reinke Mfg. Co.*, 983 F.2d 1039, 1042 (Fed. Cir. 1993). Moreover, in this particular instance, the patentee disclosed nothing else. Thus, the "video encoding means" is properly limited to this disclosed structure and its equivalents.

Accordingly, Sanyo's proposed structure of "A video signal encoder that includes a video encoder circuit implementing the MPEG1 or MPEG2 standard, a header creation circuit, and a multiplexer circuit" is the structure necessary to carry out the claimed functions.

Sub-terms

In addition, in order for the jury to understand this claim, three sub-terms "data number information," "header information" and "a predetermined video data unit" also should be construed, as none of these sub-terms have an ordinary and accustomed meaning. The specification is dispositive in this instance because the patentee defined his own terms. *Mitchell Innovations*, slip op. at 3; *Phillips*, 415 F.3d at 1316. In such situations, the inventor's lexicography governs. *Id.*

Data number information appears to be generally defined by the specification as the bit length L that is created by header creation circuit 12 and stored in the memory 3. (MT Ex. C at 4:20-25). Accordingly, the proper construction for this sub-term is: "D value indicative of the bit length of a picture, which is not part of the encoded video data."

Header information needs to be construed to place the term in the proper context. There are many different headers at issue. The specification describes the relevant headers as including: "the sequence headers, GOP headers and picture headers." (MT Ex. C at 4:23-25). Each of these headers defines the beginning of different units of video (e.g., the GOP header

defines the beginning of a GOP). Accordingly, the proper construction for this sub-term is: "Data that carries information about various parts of the encoded video data which defines the beginning of the predetermined video unit.**"** The specification teaches that the data number information and the header information are stored in the memory 3 (and referred to collectively as "the video information"). (MT Ex. C at 4:23-25).

Predetermined video data unit describes "a unit of a collection of a plurality of pictures knows as group of pictures (GOP) as shown in FIG. 3. This is for providing accessing entry points to realize random access. The GOP structure may be configured arbitrarily with the use of I, P and B pictures." (MT Ex. C at 1:34-39). Accordingly, the proper construction for this sub-term is: "A predetermined group of pictures (GOP) that can include one or more pictures."

2. Audio encoding means … (Claims 1 and 7)

The parties agree that this claim term should be construed under 35 U.S.C. § 112(6).

Function

MediaTek revised its construction and proposes that the function of this term be construed as, "encoding an audio signal into audio data to generate encoded audio data." Sanyo does not dispute the revised construction.

Structure

With regard to the structure, however, the parties still disagree in two respects. MediaTek argues that the structure should simply be an "audio signal encoder and equivalents," thereby ignoring the specification. MediaTek incorrectly asserts that there is no support in the specification for Sanyo's construction that the audio signal encoder must be a separate device from the video encoder. MediaTek is wrong. The structure should be construed as "an audio

signal encoder that is separate from the video signal encoder circuit and that implements audio compression according to the MPEG standard."

The specification of the '356 patent clearly describes a system having: "a video signal encoder 1; an audio signal encoder 2; a multiplexer 7 having memory 3 . . . , a processor 4, a header information memory 5 and a multiplexer 6; and a system data buffer 8." (MT Ex. C at 3:43-48). This description, and accompanying Figure 1, describe and show 4 separate and distinct circuits – video encoder 1, audio encoder 2, multiplexer 7 and buffer 8. In fact, the specification describes detailed circuit elements that are found within multiplexer 7, as well as detailed circuit elements that are within video signal encoder 1. The specification, however, does not suggest or otherwise describe any instance in which a single circuit would be used to perform both video signal encoding and audio signal encoding, or any instance where audio encoder 2 could be a part of video encoder 1 or multiplexer 7. Accordingly, Sanyo's proposed construction for the structure of this term requiring that the audio signal encoder is separate from the video signal encoder is proper.

The other point of dispute relates to whether the invention requires the use of circuitry that compresses the audio signals during processing. MediaTek cites to the correct portion of the specification, but draws the wrong conclusion – "Meanwhile, an audio signal input to the audio signal encoder 2 *is compressed* thereby according to the MPEG standard. The *compressed* video and audio data . . ." (MT Ex. C at 4:26-28). That citation is the one and only place in the specification where the '356 patent discusses the algorithms used to process audio signals. There is absolutely no disclosure of a single instance where audio signals are processed without being compressed. Thus, the encoding algorithm used to apply the MPEG standard, which requires compression, to audio encoding is part and parcel of the corresponding structure

identified in the '356 patent. *See WMS Gaming, Inc.*, 184 F.3d at 1349 ("In a means-plus-function claim in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm."); *see also supra* at 5.

It matters not that the patentee called this structure an "embodiment" or "example." For purposes of construing the claim under 35 U.S.C. § 112(6), this structure is the only "audio encoding means" structure in the specification that is capable of performing the claimed function. "Section 112 ... permits means-plus-function language in a combination claim, but with a 'string attached.' The 'attached string' limits the applicant to the structure, material, or acts in the specification and their equivalents." *Valmont Indus.*, 983 F.2d at 1042. Moreover, in this particular instance, the patentee disclosed nothing else. Thus, the "audio signal encoding means" is properly limited to this disclosed structure and its equivalents.

Accordingly, Sanyo respectfully requests that the Court adopt Sanyo's proposed structure of "An audio signal encoder that is separate from the video signal encoder circuit and that implements audio compression according to the MPEG standard."

3. System header generating means (Claim 1)

The parties agree that this claim term should be construed under 35 U.S.C. § 112(6).

Function

MediaTek revised its construction and proposes that the function of this term be construed as: "generating system headers on the basis of the header information and the data number information stored in the first memory."

MediaTek's proposed construction for this term is yet another attempt at obtaining an overly broad construction that is completely divorced from the patent specification.

As such, it must be rejected. *Phillips*, 415 F.3d at 1315-16 (claims "do not stand alone" and "'***must be read in view of the specification***, of which they are a part'") (citation omitted).

The essence of the invention of the '356 patent is that the prior art method of extracting video header information from the bit stream "can be eliminated, thus reducing the load of the processor." (MT Ex. C at 2:64 – 3:4). Looking to the specification as the "primary basis for construing the claims," enables a construction based on the proper ***context***. *Phillips*, 415 F.3d at 1315-16 (internal citations omitted).

Accordingly, Sanyo's contends that the function for this means-plus-function claim term is: "generating a complete system header based on the header information and data number information stored in the first memory without extracting the video header information from the bit stream."

MediaTek argues that the specification does not support Sanyo's proposed construction. MediaTek is wrong. The specification describes how the processor reads the video information (i.e., the bit length L and the sequence headers, GOP headers and picture headers) from the memory 3 "and creates the system header information for making a layered system structure." (MT Ex. C at 4:51-54). When the processor 4 has completed creating the system header, it "writes the created system header in the header information memory 5." (*Id.* at 5:10-11). This is the only suggestion or teaching of creating the system header in the '356 patent. As such, abandoning it as MediaTek argues, would eviscerate the claimed invention.

Structure

For the structure necessary to carry out the claimed function, Sanyo does not dispute MediaTek's proposed construction.

4. Multiplexing means (Claims 1 and 7)

The parties agree that this claim term should be construed under 35 U.S.C. § 112(6).

Function

Sanyo does not dispute MediaTek's revised construction of the function of this term.

Structure

With regard to the structure, however, the parties still disagree in one respect. MediaTek argues that the structure could be either a "multiplexer or a multiplexer circuit, and equivalents," once again ignoring the language of the claim itself and the specification. MediaTek incorrectly suggests that "the specification discloses the use of a multiplexer *or* a multiplexer circuit." (MT Br. 36). MediaTek is wrong. Sanyo contends that the proper construction for the structure of the term multiplexing means: "a discrete multiplexer circuit."

The specification only discloses the use of multiplexer circuit 6 (which is shown in Figure 1 as a 4-to-1 multiplexer circuit) alone to perform the multiplexing operation. (MT Ex. C at 5:23-25). If the claim were construed as MediaTek proposes, that is to include a generic "multiplexer" in addition to the multiplexer circuit, other claim terms would be superfluous. *See Philips*, 415 F.3d at 1323 (noting that claim limitations should be read in the context of the claim). If the claim were construed to include a "multiplexer," then multiplexer 7 which is described in the specification and shown in Figure 1 would be relevant. Because multiplexer 7 includes various other elements of the claim, such as the system header generating means, the first and second memories and multiplexer circuit 6, MediaTek's proposed construction would render those elements superfluous. Finally, the patentee specifically defined the processor as separate from the multiplexer circuit, in its arguments to the patent office, "This arrangement

allows the present invention to process the header information and the data number information *separately* from the multiplexing operation." (Ex. 8 at 10).

Accordingly, Sanyo respectfully requests that the Court adopt Sanyo's proposed construction for the structure of the term multiplexing means: "a discrete multiplexer circuit."

5. System header (Claims 1, 4 and 7)

MediaTek's proposed construction for the term "system header" is, in essence, to ignore the word "system," and is technically inaccurate. MediaTek's proposed construction: "Data that carries information about the audio and video streams" relies on a misreading of the specification and a dictionary definition of the term "header," not system header. While it is true that, in general, a header is the continuous control bits preceding a frame, packet or block or other data stream of bits, that definition is only appropriate for the other types of headers referred to in the specification of the '356 patent, namely, the sequence headers, GOP headers and picture headers.

The system header, on the other hand, is not associated with any specific frame, packet, etc. of data because it is essentially the detailed roadmap of how the input video will be stored as a file, once the process is complete. The specification clearly states that "The processor 4 writes the created system header in the header information memory 5." After "writing the system header information in the header information memory 5, [the processor 4] informs the multiplexer circuit 6 of information on packet formation to cause the multiplexer circuit 6 to start its multiplexing operation." (MT Ex. C at 5:10-16).

Accordingly, the term <u>"system header" should be construed as:</u>

<u>"A complete data structure that is combined with the combined encoded video and audio data streams."</u>

V. CONCLUSION

In view of the foregoing, Sanyo respectfully requests that the Court adopt Sanyo's proposed claim constructions.

Dated: September 15, 2006

Respectfully submitted,

By: */s/ John F. Bufe*

MICHAEL E. JONES, Lead Attorney
Texas State Bar No. 10929400
JOHN F. BUFE
Texas State Bar No. 03316930
POTTER MINTON
110 North College
500 Plaza Tower (75702)
P.O. Box 359
Tyler, Texas 75710
Telephone: (903) 597-8311
Facsimile: (903) 593-0846
Email: mikejones@potterminton.com
Email: johnbufe@potterminton.com

**ATTORNEYS FOR DEFENDANTS
SANYO ELECTRIC CO., LTD., and
SANYO NORTH AMERICA CORPORATION**

Of Counsel:
Patricia A. Martone
Robert W. Morris
Hiroyuki Hagiwara
Andrew Oliver
Padmaja Chinta
ROPES & GRAY LLP
1251 Avenue of the Americas
New York, NY 10020
Telephone: (212) 596-9000
Facsimile: (212) 596-9090
Email: patricia.martone@ropesgray.com

Attorney For Defendants
**Sanyo Electric Co., Ltd, and
Sanyo North America Corp.**

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a). As such, this notice was served on all counsel who have consented to electronic service. Local Rule CV-5(a)(3)(A). Pursuant to Fed. R. Civ. P. 5(d) and Local Rule CV-5(e), all other counsel of record not deemed to have consented to electronic service were served with a true and correct copy of the foregoing by U.S. mail, on this the 15th day of September, 2006.

/s/ John F. Bufe
John F. Bufe

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